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PRODUCT NOTE

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GPC_5A1 - LCD DRIVER

INTRODUCTION

The GPC_5A1 is a small general purpose Liquid Crystal Display control module. It was designed to be connected to the CPU_1A1 (HC11F1 CPU module), but can easily be used with any other microprocessor or microcontroller.

It's purpose is to interface a standard parallel LCD module to a CPU without taking up a lot of CPU or I/O resources. The same interface and driver routines can be used to attach other I/O modules.

A key feature of the GPC_5A1 is the 3-wire bus. This is a master-slave system. The GPC_5A1 is a slave that is controlled from a master device, normally a CPU_1A1 module or your own system. This allows a number of similar I/O modules to be connected to the same 3-pins of the controlling device, thus providing significant I/O expansion for the loss of only 3 pins. This system allows I/O devices to interrupt the master when required, providing rapid input response by eliminating the need for polling of I/O devices.

The GPC_5A1 will support alphanumeric LCD modules of up to 4-line by 40-character in size.

The GPC_5A1 supports LED back-lighting. This is activated for 2 minutes whenever data is sent to the display. It can also be command controlled. Because LED back-lighting requires quite a high current at a lower voltage, PWM is used to minimize the power loss and reduce the average current drain.

AVAILABILITY & APPLICATION

Availability

PMB Electronics supplies the GPC_5A1 as a pre-programmed CHIP and as a working PCB module. Sample Master code is provided for the HC11.

PMB Electronics can also supply suitable LCD modules and interconnect cables. See www.pmb.co.nz for additional information and current pricing.

Application

To apply the GPC_5A1 you need a minimum of 3 available I/O pins on your project /product or application CPU (the master). One of these can be the IRQ input or any other pin with interrupt capability.

Note that the interrupt is not essential, but does improve input response when using input modules (not required when using just the GPC_5A1).

The clock pin on the master need only be an output pin. The data pin must be bi-directional (input and output).

The LCD module connects to the GPC_5A1, and the GCP_5A1 connects to the master. A couple of support routines run on the master looking after transmission to the slave and reception from the slave. Reception can be interrupt initiated on the master.

The processing time required on the master varies with message length. Being synchronous means that the master can multitask transmission and reception. The timeout period of the slave of 10mS must not be exceeded between bits. Messages being sent to the slave can be broken into smaller segments and sent as processing time permits.

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Generally the GPC_5A1 slave will be located close to the master; in the same box. The slave can be operated at some distance from the master; 20 meters or more. This requires a better interface between the master and the 3-wire bus. A suitable circuit is provided with the GPC_5A1 PCB module. This format requires 4-pin connection to the master due to the data line being split into transmit and receive in order to add a driver and receive buffer.

3-WIRE BUS

The 3-wire PMBUS4 allows simple I/O expansion modules to be parallel connected to a controlling device or master. The expansion modules are slaves. The master provides a clock for all data transfers to and from the slaves. The slaves can interrupt the master when there is something to report. This ability must be enabled. By default the slaves will not interrupt the master.

The bus consists of 3 wires and ground. Often a +ve power line will also be included:

1.	+ve	+12V power line	.
2.	0V	ground reference, power	.
3.	interrupt I/O		active low
4.	data	I/O	bi-directional
5.	clock	from master	0 to 1 = clock

Each slave device has a family-code and a unit-ID code. The family code allows all devices of the same type to be addressed as a group. The unit-ID allows multiple slaves of the same family-code to be individually addressed. Both family and ID codes are 8 bits long each.
A family-code of 00h is read as a valid code, allowing all devices to be addressed at once, a family broadcast. If the unit-ID is also 00h all slaves on the network will act on the command. A specific family-code and a unit-ID of 00h allows a command to be accepted by all slaves of the same family-code. The family and ID codes installed in each slave can only be changed at assembly time.

The interrupt line is normally high, going low to get the attention of the master, staying low during the transmission from the slave. This indicates to other slaves that the bus is in use and not to transmit. The master must be set to accept the interrupt as an edge detected input, not a level sensitive input.

The clock line is normally low. It is always driven by the master. Slaves use the clock to synchronize reading from and transmitting on the data line.

The data line toggles high and low as required, in sync with the clock line. The data line can be driven by the master or the slave depending on the direction of communication.

COMMUNICATIONS

The PMBUS4 interrupt line is used to get the attention of the master and to indicate to other slaves that the bus is in use. At the slave, the interrupt line is an input until required. It is then switched to be an output and held low for the duration of the transmission to the master. If the interrupt is already low, it means that another slave module is currently transmitting on the bus. This slave waits until the interrupt line is clear before proceeding.

All slaves receive all messages. This prevents a slave from transmitting while the master is transmitting. On reception of a complete message, the checksum, family-code and unit-ID are
checked. If all are correct, the new message is processed.

The maximum message length is determined by the available buffer memory. This is set to 28 bytes in the PIC16C711 and PIC16F84.

The message format is:

; F T F B C D . . . . . .K

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; family-code, to, from, byte-count, command, data . . . .checksum

This allows a maximum of 23 bytes of actual message data.

NOTES:

- The master clocks data in both directions.
- Bits are transmitted MSB first, clocked by the master.
- Bits are transmitted non-inverted ie. logic 1 = +ve on the data line.
- The slave detects the rising edge of the interrupt, which results in the next bit being placed on the data line.
- The slave detects the rising edge of the clock and reads the next bit from the data line.
- The checksum is the value required to make all other bytes added = zero.

COMMANDS

The commands supported by the GPC_5A1 are listed here:

C4	write address	(raw address)		2 data	yes
C8	reset	(cold restart)		0 data	yes
CE	master interrupt mode	(disable)	0 data	yes	
D1	back-light on	.		0 data	yes
D2	back-light off	.		0 data	yes
D3	clear display	.		0 data	yes
D4	restore display	.		0 data	yes
D5	set LCD char. Address	.	1 data	yes	
D6	write command to LCD	.	1 data	yes	
D7	display data on LCD	(10 bytes max)		? data	yes
D8	use E1 (upper half)	.		0 data	yes
D9	use E2 (lower half)	.		0 data	yes
DA	use E1 & E2 (both	.		0 data	yes

DETAILS

- Description = LCD display controller
- Family Code = 22h ($22)
- Unit ID = 01h ($01)
- Communication = 3-wire serial bus (PMBUS4)
- CPU = PIC16C711-04
- LCD mode = 4 bit
- Back-light = PWM LED
- Power = 12V nominal (on-board regulator)

CONNECTIONS

LCD Connection

Conection to LCD module is via the 20 way header.
Pin-1 is at the same end as the contrast control.

pin	function	4x20	4x40

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1	n.c.		-	-	
2	enable #2		-	y	
3	VSS (0V)		y	y	
4	VDD (+5V)		y	y	
5	contrast voltage	y	y		
6	RS		y	y	
7	R/W		y	y	
8	enable #1		y	y	
9	spare (not used)	-	-		
10	n.c.		-	-	
11	n.c.		-	-	
12	n.c.		-	-	
13	D4		y	y	
14	D5		y	y	
15	D6		y	y	
16	D7		y	y	
17	LED back-light +ve		y	-	**CAUTION**, see note below
18	LED back-light -ve		y	-	
19	n.c.		.	.	
20	n.c.		.	.	

NOTE:

- The backlight connections (pins 17 &18) are referenced to +12V. Ensure that these are not accidentally connected to any of the other LCD lines.

BUS Connection

1	+ve	+12V power line	.
2	0V	ground reference, power	.
3	interrupt	I/O	active low
4	data	I/O	bi-directional
5	clock	from master	0 to 1 = clock

CUSTOMISATION

By changing the Unit-ID, more than one GPC_5A1 can be placed on the same 3-wire bus and operated independently. PMB Electronics can produce GPC_5A1 controllers with changed Unit-ID numbers as required.